

1-4 submitted herewith. The Applicants are concurrently submitting a Letter Submitting Drawings and a Letter to the Examiner Requesting Approval of the Changes to the Drawings. The Applicants respectfully request that the Examiner withdraw the objections thereto.

**Support for Claim Amendments:**

Support for the amendments to claims 1 and 5 may be found in the Specification at Figure 6 and at page 10, line 15 through page 11, line 2.

**Rejections Under 35 U.S.C. § 102(b):**

Nishiyama discusses automated design of an LSI (Nishiyama, col. 2, lines 34-35).

Claims 1 and 5 of the subject application (as amended herein) recite "obtaining second design data of a rank of hierarchy higher than the predetermined rank of hierarchy, after the obtaining the first design data."

In the general technical field of hierarchical circuit design, it is common to refer to a lower rank when an upper rank is referred to. Nishiyama discusses such a common scheme. Generally, in this technical field, a hierarchical expression is made such that lower ranks are expressed from an upper rank in a try expression manner. Accordingly, when an upper rank is referred to, lower ranks are referred to at the same time, generally.

In contrast, in the present invention, when a lower rank is referred to, data of an upper rank, which is physical data that is present in the lower rank physically, can be selectively referred to, after referring to the lower rank. Nishiyama does not disclose or suggest the same. Nishiyama, in the section cited by the Examiner, only discusses selecting a lower rank at the same time as when an upper rank is selected (Nishiyama, col. 20, lines 61-64). Therefore, claims 1 and 5 of the subject application (as amended herein) patentably distinguish over Nishiyama.

**New Claim 9:**

New claim 9 is added herein. Support for new claim 9 may be found in the Specification at Figure 6 and at page 10, line 15 through page 11, line 2.

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New claim 9 recites "retrieving wiring data of an upper rank from the storage unit, after the retrieving the design data." In contrast, as discussed above, Nishiyama does not disclose or suggest the same. Therefore, claim 9 is patentably distinguishable over Nishiyama.

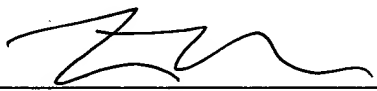
Withdrawal of the foregoing rejections is respectfully requested.

There being no further objections or rejections, it is submitted that the application is in condition for allowance, which action is courteously requested. Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters. If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

Please AMEND claims 1 and 5. The remaining claims are reprinted, as a convenience to the Examiner, as they presently stand before the U.S. Patent and Trademark Office.

1. (ONCE AMENDED) A design data processing method of processing hierarchically configured design data, comprising [the steps of]:
- [a] ]obtaining first design data of a predetermined rank of hierarchy;
  - [b] ]obtaining second design data of a rank of hierarchy higher than the predetermined rank of hierarchy, after the obtaining the first design data; and
  - [c] ]combining the second design data to the first design data.

2-4. (CANCELED)

5. (ONCE AMENDED) A computer readable recording medium storing a software program for processing hierarchically configured design data, which when executed by a computer, cause the computer to perform operations comprising: [and causing a computer to execute the following steps of:]

- [a] ]obtaining first design data of a predetermined rank of hierarchy;
- [b] ]obtaining second design data of a rank of hierarchy higher than the predetermined rank of hierarchy, after the obtaining the first design data; and
- [c] ]combining the second design data to the first design data.

6-8. (CANCELED)

Please ADD the following new claims:

9. (NEW) A method of designing a hierarchical layout of a circuit, comprising:
- receiving a designation of a specified rank from a user;
  - retrieving design data of the specified rank from a storage unit;
  - retrieving wiring data of an upper rank from the storage unit, after the retrieving the design data;

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setting the wiring data in the design data; and  
displaying the design data in which the wiring data has been set on a display unit.

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